CLAIMS

1. A phase control loop circuit for tuning to a reference frequency signal comprising:

a phase lock loop (PLL) circuit being responsive to a reference frequency signal having a reference frequency, said PLL circuit including a voltage control oscillator (VCO) for generating a VCO output, said PLL circuit for generating a PLL output, said phase control loop circuit processing said VCO output to generate an output frequency signal having an output frequency; and

a coarse tuning circuit being coupled to said PLL circuit, said coarse tuning circuit being responsive to said PLL output for processing the same to generate a counter output, said VCO being responsive to said counter output, said counter output being used for coarse tuning said output frequency signal to said reference frequency signal, said coarse tuning circuit further responsive to a lock detection (LD) signal, said LD signal for controlling said counter output to cause said output frequency to be within a predetermined range of frequencies including said reference frequency, said PLL circuit for fine tuning said output frequency signal to said reference frequency signal,

wherein said PLL circuit and said coarse tuning circuit tune the output frequency to a reference frequency included in a wide range of frequencies.

2. A phase control loop circuit as recited in claim 1 wherein said PLL circuit includes a phase-frequency detector (PFD) circuit for comparing said output frequency with said reference frequency to generate a PFD output, said PFD output including a Δf signal for representing the difference between said output frequency and said reference frequency.

3. A phase control loop circuit as recited in claim 2 wherein said PLL circuit further includes a charge pump (CP) circuit responsive to said PFD output for generating a current, the value of said current being based on the value of said Δf signal.

4. A phase control loop circuit as recited in claim 3 wherein said PLL circuit further includes a loop filter responsive to said current for converting the same to generate a control voltage (V_{ctrl}) signal having a voltage value V_{ctrl}, said V_{ctrl} signal being provided to said VCO to control said VCO output, said V_{ctrl} signal controlling said VCO output to enable said PLL circuit to fine tune said output frequency to said reference frequency.

5. A phase control loop circuit as recited in claim 1 further including a divider circuit responsive to said VCO output for dividing the same by a factor N to generate said output frequency signal.

6. A phase control loop circuit as recited in claim 4 wherein said coarse tuning circuit includes a comparator circuit, said comparator circuit including a first comparator and a second comparator, said V_{ctrl} signal being included in said PLL output, said first and second comparators being responsive to said PLL output, said first comparator being responsive to a first fixed value signal having a first voltage value, said second comparator being responsive to a second fixed value signal having a second voltage value.

7. A phase control loop circuit as recited in claim 6 wherein said first voltage value is two thirds of a predetermined voltage value (V_{cc}), said second voltage value is one third of said V_{cc}.

8. A phase control loop circuit as recited in claim7 wherein said first comparator for comparing said V_{ctrl} to said first voltage value, said second comparator for comparing said V_{ctrl} to said second voltage value, said first comparator for generating a first comparator output and said second comparator for generating a second comparator output.

9. A phase control loop circuit as recited in claim 8 wherein said coarse tuning circuit further includes a counter control circuit, said counter control circuit including a first nand gate and a second nand gate responsive to said first comparator output, said first nand gate being responsive to said second

comparator output, said second nand gate being responsive to an inverted version of said second comparator output.

10. A phase control loop circuit as recited in claim 9 wherein said coarse tuning circuit further includes a counter for generating a counter output, the output of said first nand gate causes said counter to count, the output of said second nand gate causes said counter output to be maintained.

11. A phase control loop circuit as recited in claim10 wherein said counter being responsive to the output of a third nand gate, said third nand gate being responsive to a lock detection (LD) signal and a clock signal, said clock signal provides clock cycles to said counter wherein at each said clock cycle said counter begins to count, said LD signal for overriding said clock signal to halt the counting performed by said counter.

12. A phase control loop circuit as recited in claim 8 wherein said VCO has a positive polarity, said V_{ctrl} being less than said second voltage value causes said counter to count up to increase said counter output, said V_{ctrl} being greater than said first voltage value causes said counter to count down to decrease said counter output, said V_{ctrl} being greater than said second voltage value and less than said first voltage value causes said second counter to stop counting and maintain said counter output, said V_{ctrl} being greater than said second voltage value and less

than said first voltage value causes said output frequency to be within said predetermined range of frequencies.

13. A phase loop control circuit as recited in claim 10 wherein said counter is a 4-bit counter, said counter enabling said phase control loop circuit to tune said output frequency to said reference frequency included in an increased range of frequencies.

14. A phase control loop circuit as recited in claim 1 included within a receiver for receiving radio frequency (RF) signals, said receiver further including a low noise amplifier responsive to said RF signals for generating amplified RF signals, said receiver further including a mixer responsive to said amplified RF signals and said VCO output for converting said amplified RF signals to baseband signals.

15. A phase control loop circuit as recited in claim 11 wherein said PLL circuit is essentially an analog circuit, said LD signal for preventing jitter generated by said comparator circuit to affect said PLL circuit.

16. A phase control loop circuit as recited in claim 14 for tuning to said reference frequency included in a wide range of frequencies to compensate for the process variations caused by manufacturing said receiver.

17. A phase control loop circuit as recited in claim 1 wherein said PLL circuit and said coarse tuning circuit cause said output frequency signal to have essentially the same phase as said reference frequency signal.

18. A phase control loop circuit as recited in claim 1 wherein said PLL circuit and said coarse tuning circuit tune said output frequency to said reference frequency on-the-fly.

19. A method for tuning to a reference frequency signal comprising:
receiving the reference frequency signal having a reference frequency;
generating a voltage control oscillator (VCO) output;
generating a phase lock loop (PLL) output;
processing the VCO output to generate an output frequency signal having an output frequency;
processing the PLL output to generate a counter output;
coarse tuning the output frequency signal to the reference frequency signal;
receiving a lock detection (LD) signal; and
controlling the counter output to cause the output frequency to be within a predetermined range of frequencies; and
fine tuning the output frequency signal to the reference frequency signal, wherein the output frequency is tuned to the reference frequency included in a wide range of frequencies.

20. A phase control loop circuit for tuning to a reference frequency signal comprising:

means for receiving the reference frequency signal having a reference frequency;

means for generating a voltage control oscillator (VCO) output;

means for generating a phase lock loop (PLL) output;

means for processing the VCO output to generate an output frequency signal having an output frequency;

means for processing the PLL output to generate a counter output;

means for coarse tuning the output frequency signal to the reference frequency signal;

means for receiving a lock detection (LD) signal; and

means for controlling the counter output to cause the output frequency to be within a predetermined range of frequencies; and

means for fine tuning the output frequency signal to the reference frequency signal, wherein the output frequency is tuned to the reference frequency included in a wide range of frequencies.